What is claimed is:

1. A method of forming poly-silicon thin film transistors, comprising the steps of:

providing an amorphous silicon thin film transistor; and

heating the amorphous silicon thin film transistor with an IR to change the amorphous silicon thin film transistor into a poly-silicon thin film transistor.

2. The method of claim 1, wherein the amorphous silicon thin film transistor comprises a bottom-gate or top-gate structural type.

3. The method of claim 2, wherein the bottom-gate structural type comprises a back channel etch (BCE) or a channel protect (CHP) structural type.

4. The method of claim 3, wherein forming the back channel etch (BCE) structural type comprises steps of:

forming a gate metal on a substrate;

forming a gate insulator, an amorphous silicon layer, and a doped amorphous silicon layer in turn on the gate metal and the substrate simultaneously;

patterning the amorphous silicon layer and the doped amorphous silicon layer to form an active layer region;

forming a source/drain metal on the doped amorphous silicon layer;

patterning the source/drain metal to form a data line; and

patterning the doped amorphous silicon layer to define a channel region.

5. The method of claim 3, wherein forming the channel protect (CHP) structural type comprises steps of:

forming a gate metal on a substrate;

forming a gate insulator, an amorphous silicon layer, and a protective layer in turn on the gate metal and the substrate simultaneously;

patterning the protective layer to form an etching stop layer;

forming a doped amorphous silicon layer on the amorphous silicon layer and the etching stop layer;

patterning the amorphous silicon layer and the doped amorphous silicon layer to form an active layer region;

forming a source/drain metal on the doped amorphous silicon layer;

patterning the source/drain metal to form a data line; and

patterning the doped amorphous silicon layer to define a channel region.

6. The method of claim 2, wherein forming the top-gate structural type comprises steps of:

forming a buffer layer on a substrate;

forming an amorphous silicon layer on the buffer layer;

forming a gate insulator on the amorphous silicon layer;

forming a gate metal on the gate insulator;

utilizing the gate metal as a mask to ion implant the amorphous silicon layer on two sides of the gate metal for defining a source/drain region in the amorphous silicon layer;

forming a dielectric interlayer on the gate metal and the gate insulator;

patterning the dielectric interlayer to form contact holes;

forming a source/drain metal on the dielectric interlayer and in the contact holes to connect the source/drain region in the amorphous silicon layer; and

patterning the source/drain metal to form a data line.

7. The method of claim 1, wherein the step of heating with the IR comprises a pulsed rapid thermal processing (PRTP) technology.

8. A method of forming poly-silicon thin film transistors employed for flat panel display, comprising the steps of:

forming a gate metal on a substrate;

forming a gate insulator, an amorphous silicon layer, and a doped amorphous silicon layer in turn on the gate metal and the substrate simultaneously;

patterning the amorphous silicon layer and the doped amorphous silicon layer to form an active layer region;

forming a source/drain metal on the doped amorphous silicon layer;

patterning the source/drain metal to form a data line;

patterning the doped amorphous silicon layer to define a channel region; and

performing a heating process with an IR, wherein the gate metal and the source/drain metal rapidly absorb heat energy from the IR and transfer the heat energy to the amorphous silicon layer, and the amorphous silicon layer subsequently crystallizes to become a poly-silicon layer.

9. The method of claim 8, wherein the gate metal is a metal material with good IR absorption and thermal stability.

10. The method of claim 9, wherein the metal material comprises chromium (Cr) or moly-tungsten (MoW).

11. The method of claim 8, wherein the source/drain metal is a metal material with good IR absorption and thermal stability.

12. The method of claim 11, wherein the metal material comprises chromium (Cr) or moly-tungsten (MoW).

13. The method of claim 8, wherein the heating process with the IR comprises a pulsed rapid thermal processing (PRTP) technology.

14. A method of forming poly-silicon thin film transistors employed for flat panel display, comprising the steps of:

forming a buffer layer on a substrate;

forming an amorphous silicon layer on the buffer layer;

forming a gate insulator on the amorphous silicon layer;

forming a gate metal on the gate insulator;

utilizing the gate metal as a mask to ion implant the amorphous silicon layer on two sides of the gate metal for defining a source/drain region in the amorphous silicon layer;

forming a dielectric interlayer on the gate metal and the gate insulator;

patterning the dielectric interlayer to form contact holes;

forming a source/drain metal on the dielectric interlayer and in the contact holes to connect the source/drain region in the amorphous silicon layer;

patterning the source/drain metal to form a data line; and

performing a heating process with an IR, wherein the gate metal and the source/drain metal rapidly absorb heat energy from the IR and transfer the heat energy to the amorphous silicon layer, and the amorphous silicon layer subsequently crystallizes to become a poly-silicon layer.

15. The method of claim 14, wherein the gate metal is a metal material with good IR absorption and thermal stability.

16. The method of claim 15, wherein the metal material comprises chromium (Cr) or moly-tungsten (MoW).

17. The method of claim 14, wherein the dielectric interlayer comprises a silicon nitride layer or a silicon oxide layer.

18. The method of claim 14, wherein the source/drain metal is a metal material with good IR absorption and thermal stability.

19. The method of claim 18, wherein the metal material comprises chromium (Cr) or moly-tungsten (MoW).

20. The method of claim 14, wherein the heating process with the IR comprises a pulsed rapid thermal processing (PRTP) technology.